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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/853,769	05/14/2001	Takashi Hotta	500.28166CX2	7218

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EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 08/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/853,769	HOTTA ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-40* is/are pending in the application.

4a) Of the above claim(s) *1-16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 07/433,368.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 17-40 remain for examination. Claims 1-16 have been canceled.

2. Applicant's arguments filed on 06/07/05 with respect to claims 17-40 have been considered but are moot in view of the new ground(s) of rejection.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 17-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeGroot (4,766,564) in view of Chevillat (4,615,004).

4. As to claims 17,18, 23-25, DeGroot taught a system comprising at least :

a) a register for storing data (see fig.1);

b) a plurality of arithmetic operation units to execute plurality of instructions stored in memory in parallel (see fig.1 , ADD, MUL);

c) a plurality of signal lines for sending data stored in the register to an arithmetic unit (see the output connection 22,24 of the register to the input of ADD and MUL in fig . 1) ;

d) a second plurality of signal lines for storing result data from the arithmetic units in register (see output of ADD and MUL to the input of register in fig.1):

e) a bypass circuit (adder bypass bus and mul bypass bus) for connecting the first and

second plurality of signal lines to use data resulting from the arithmetic output for next cycle (see fig.1, see the bypass bus with the switches from the arithmetic units to the instruction , see the control input of the arithmetic units), the bypass being controlled by ns of arithmetic instructions in col.3, lines 1-46, see fig.3, see also col.5, lines 17-42 for bypass cycle).

5. DeGroot did not specifically showed the fetching of the plurality of instructions at one time as claimed. However, Chevillat disclosed a system for fetching plurality of instructions in parallel (see the instructions fetched in single machine cycle in col.7, lines 32-39). It would have been obvious to one of ordinary skill in the art to use Chevillat in DeGroot for including the fetching of plurality of instructions at one time as clamed because the use of Chevillat could provide DeGroot the capability to schedule the processing of instructions in greater number at a given time, thereby increasing the bandwidth of the instruction processing, and it could be readily achieved by configuring the fetching unit of Chevillat into DeGroot with modified system parameters (such as the instruction width, and instruction number) so that the fetching of plurality instructions could be recognized by DeGroot at a predetermined fetching cycle, and because DeGroot also taught that a greater number of instructions could be executed in a single cycle for faster operation speed (see col.1, lines 11-20) , which was suggestion of the need for fetching more instructions in a given time in order to adapt to faster execution speed , and in doing so , provided a motivation.

DeGroot is used as primary reference because it shows the detailed structure of the bypass circuit and connections of plurality of switches. Chevillat is used to supplement the teaching of the fetching instructions in parallel or at one time.

6. As to claims 19, 20, DeGroot also included switches (see the switches in fig.3).

7. As to claim 21 , 22 , DeGroot disclosed a system including at

a) a register for storing data (see fig.1);

b) a plurality of arithmetic operation units to execute plurality of instructions stored in memory in parallel (see fig.1, ADD, MUL);

c) a plurality of signal lines for sending data stored in the register to an arithmetic unit (see the output connection 22,24 of the register to the input of ADD and MUL in fig . 1) ;

d) a second plurality of signal lines for storing result data from the arithmetic units in register (see output of ADD and MUL to the input of register in fig.1);

e) a plurality of switches (see the switches with the adder bypass bus and mul bypass bus in fig.3) for connecting the first and second plurality of signal lines to use data resulting from the arithmetic output for next cycle (see fig.1, see the bypass bus with the switches from the arithmetic units to the input of the arithmetic units), the bypass being controlled by instructions see the control of arithmetic instructions in col.3, lines 1-46, see fig.3).

8. DeGroot did not specifically showed the fetching of the plurality of instructions at one time as claimed. However, Chevillat disclosed a system for fetching plurality of instructions in parallel (see the instructions fetched in a single machine cycle in col.7,

lines 32-39). It would have been obvious to one of ordinary skill in the art to use Chevillat in DeGroot for including the fetching of plurality of instructions at one time as clamed because the use of Chevillat could provide DeGroot the capability to schedule the processing of instructions in greater number at a given time, thereby increasing the bandwidth of the instruction processing, and it could be readily achieved by configuring the fetching unit of Chevillat into DeGroot with modified system parameters (such as the instruction width, and instruction number) so that the fetching of plurality instructions could be recognized by DeGroot at a predetermined fetching cycle, and because DeGroot also taught that a greater number of instructions could be executed in a single cycle for faster operation speed (see col.1, lines 11-20) , which was suggestion of the need for fetching more instructions in a given time in order to adapt to faster execution speed , and in doing so , provided a motivation.

DeGroot is used as primary reference because it shows the connections of the plurality of switches. Chevillat is used to supplement the teaching of the fetching instructions in parallel.

9. As to claim 26 , DeGroot also included different arithmetic operations (see the ADD and MUL in fig.3).

10. As to claims 27,28,29,30, 31-34, DeGroot also included bypass for transferring the data between the different arithmetic units (see the input.connection to the switch at each input of the arithmetic units in fig.3, see also limitations already set forth in paragraph # 3 and 5).

11. DeGroot did not specifically showed the fetching of the plurality of instructions at one time as claimed. However, Chevillat disclosed a system for fetching plurality of instructions in parallel (see the instructions fetched in single machine cycle in col.7, lines 32-39). It would have been obvious to one of ordinary skill in the art to use Chevillat in DeGroot for including the fetching of plurality of instructions at one time as clamed because the use of Chevillat could provide DeGroot the capability to schedule the processing of instructions in greater number at a given time, thereby increasing the bandwidth of the instruction processing, and it could be readily achieved by configuring the fetching unit of Chevillat into DeGroot with modified system parameters (such as the instruction width, and instruction number) so that the fetching of plurality instructions could be recognized by DeGroot at a predetermined fetching cycle, and because DeGroot also taught that a greater number of instructions could be executed in a single cycle for faster operation speed (see col.1, lines 11-20) , which was suggestion of the need for fetching more instructions in a given time in order to adapt to faster execution speed , and in doing so , provided a motivation.
DeGroot is used as primary reference because it shows the detailed structure of the bypass circuit and the connections of the plurality of switches. Chevillat is used to supplement the teaching of the fetching instructions in parallel.

12. As to claims 35,36, DeGroot also included bypass for transferring the data between the different arithmetic units and also into the register (see the input

connection to both the register input and to the switch at each input of the arithmetic units in fig.3, see also limitations already set forth in paragraph # 3,5).

13. As to the fetching of instructions at a time, see paragraph 4 for the obviousness discussions above.

14. As to claim 37, DeGroot also included at least :

a) a plurality of registers (see the register file);

b) first and second arithmetic units for execution instructions based on plurality of instructions stored in memory (see the execution of the arithmetic instructions in col.3, lines 5-46).,

c) first signal lines transferring data from registers to the first arithmetic unit (see the output 22 from the register to the ADD);

d) second signal lines transferring data from registers to second arithmetic unit (see the output 24 from registers ton the MUL in fig.3);

e) third signal fro transferring data from the first arithmetic unit (ADD) to the register (see output from ADD into registers 8 in fig.1);

f) forth signal fro transferring data from the second arithmetic unit (MUL) to the register (see output from MUL into registers 8 in fig.1);

g) the first bypass bus (see fig.1 , the bypass to the input switch of ADDI;

h) the second bypass bus (see fig.1 , the bypass to the input switch of MUL).

15. AS to the fetching of plurality of instructions at a time, see paragraph # 4 for the obviousness discussions above.

16. As to claims 38-40, see the input switches at ADD and MUL in fig.3.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Harigai et al. (4,747,045) is cited for the teaching of simultaneous fetch of plurality of instructions in one cycle (see col.5, lines 17-20).

17. DeGroot (4,766,564) was cited in the record, therfore, copy is not provided herein.

Applicant's amendment (e.g. see newly amended feature of fetching the plurality of instructions at a time in claim 1) necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

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